Amendments to the Claims:

Claims 1-6 and 10-26 (withdrawn)

Claim 7 (currently amended) An RF passive circuit comprising:

a semiconductor substrate;

a via-hole through the semiconductor substrate, the via-hole having a metal film on an inside wall;

a wiring metal layer formed in a spiral pattern with an inside end on the semiconductor substrate, the wiring metal layer being electrically connected to the via-hole at the inside end;

an inductor of metal film formed in a spiral pattern with an inside end on the wiring metal layer with the inside end of the inductor film being near the via-hole; and

a dielectric layer between the spiral wiring metal layer and the spiral inductor metal film,

wherein the spiral wiring metal layer and the spiral inductor metal film are disconnected from each other near the via-hole.

Claim 9 (currently amended) An RF choke used in at least one of a matching circuit and a bias feeding circuit, both circuits being included in an RF amplifier, the RF choke comprising:

a semiconductor substrate where at least one of the matching circuit and the bias feeding circuit is incorporated;

a via-hole through the semiconductor substrate, the via-hole having a metal film on an inside wall;

a wiring metal layer formed in a spiral pattern with an inside end on the semiconductor substrate, the wiring metal layer being electrically connected to the via-hole at the inside end;

an inductor of metal film formed in a spiral pattern with an inside end on the wiring metal layer with the inside end of the inductor film being near the via-hole; and

a dielectric layer between the spiral wiring metal layer and the spiral inductor metal film,

wherein the spiral wiring metal layer and the spiral inductor metal film are disconnected from each other near the via-hole.

Claim 27 (previously amended) The RF passive circuit of Claim 7, wherein the wiring metal layer is formed by an evaporation process.

Claim 28 (previously amended) The RF passive circuit of Claim 7, wherein the inside end of the wiring metal layer is connected to the via-hole by a ground layer over one end of the via-hole on the semiconductor substrate.